NATIONAL UNIVERSITY OF LESOTHO

B.Eng SUPPLEMENTARY EXAMINATIONS

EE3401 – Analogue Circuit Designs

August 2023 **TIME: 3 HOURS**

INSTRUCTIONS:

i) Answer any 4 questions

ii) Begin each question on a new page

TOTAL MARKS: 100

Question 1

a) i) Why is a photodiode operated in reverse bias? [4 Marks]

ii) Explain a relationship between its reverse current and the magnitude of the incident light. [2 Marks]

b) If the transistor in Figure 1 is open from collector to emitter, the voltage across *R*C will
(i) increase (ii) decrease (iii) not change [1 Mark]

c) If the transistor in Figure 1 is open from collector to emitter, the collector voltage will
(i) increase (ii) decrease (iii) not change [1 Marks]

d) If the base resistor in Figure 1 is open, the transistor collector voltage will
(i) increase (ii) decrease (iii) not change [1 Mark]

e) If the emitter in Figure 1 becomes disconnected from ground, the collector voltage will
(i) increase (ii) decrease (iii) not change [1 Mark]

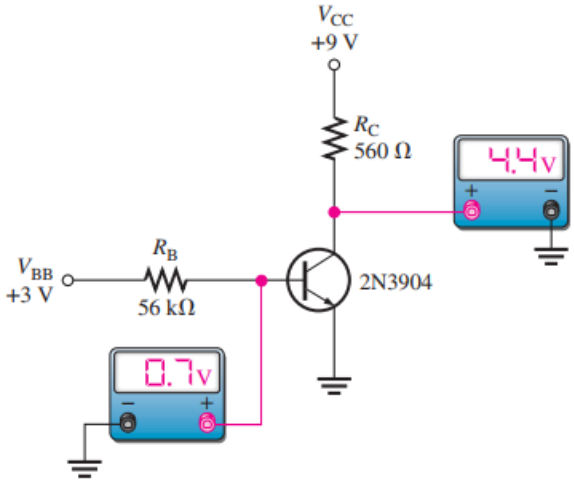

Figure 1

f) If the transistor in Figure 2 is saturated and the base current is increased, the collector current will
(i) increase (ii) decrease (iii) not change [1 Mark]

g) If R_C in Figure 2 is reduced in value, the value of $I_{C(sat)}$ will
(i) increase (ii) decrease (iii) not change [1 Mark]

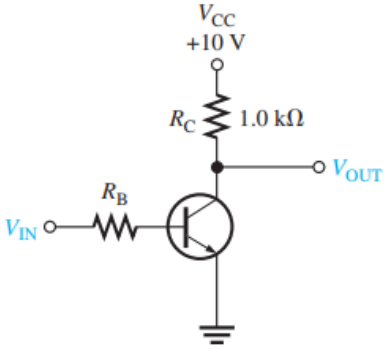

Figure 2

h) The transistor in the figure below is used as a switch to turn LED ON and OFF. The LED requires minimum of 30 mA to emit a sufficient level of light. For the following circuit values, determine the amplitude of the square wave input voltage necessary to make sure that the transistor saturates. Use double minimum value of the base current as a safety margin to ensure saturation. V_{CC} = 9V, $V_{CE(sat)}$ = 0.3V, R_C = 220 Ω, R_B = 3.3 kΩ, and β_{DC} = 50 and V_{LED} = 1.6V.
[8 Marks]

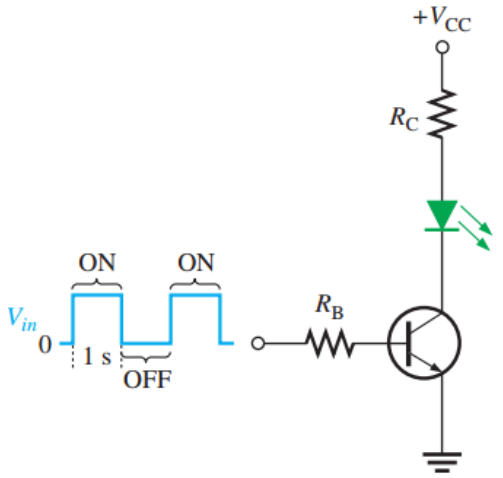

Figure 3

I) The output from a phototransistor can be used to activate or deactivate a relay. If in Figure 4 below there is no incident light, is the relay conducting or not conducting? [1 Marks]. Elaborate on your answer. [4 Marks]

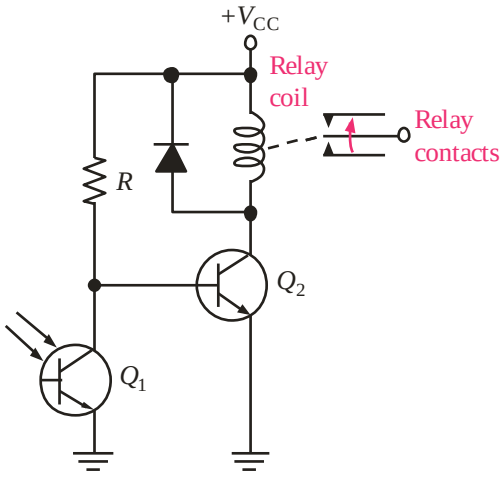

Figure 4

[Total = 25 Marks]

Question 2

a) Answer with either True or False for the following questions

(i) The two regions of a diode are the anode and the collector. [1 Mark]
(ii) When reverse-biased, a diode ideally appears as a short. [1 Mark]
(iii) The output frequency of a half-wave rectifier is twice the input frequency. [1 Mark]
(iv) The purpose of the capacitor filter in a rectifier is to convert ac to dc. [1 Mark]
(v) A smaller filter capacitor reduces the ripple. [1 Mark]
(vi) The purpose of a clamper is to remove a dc level from a waveform. [1 Mark]

b) Determine whether each diode in Figure 5 is forward biased or reverse biased and determine the voltage across each diode assuming the practical model. [8 Marks]

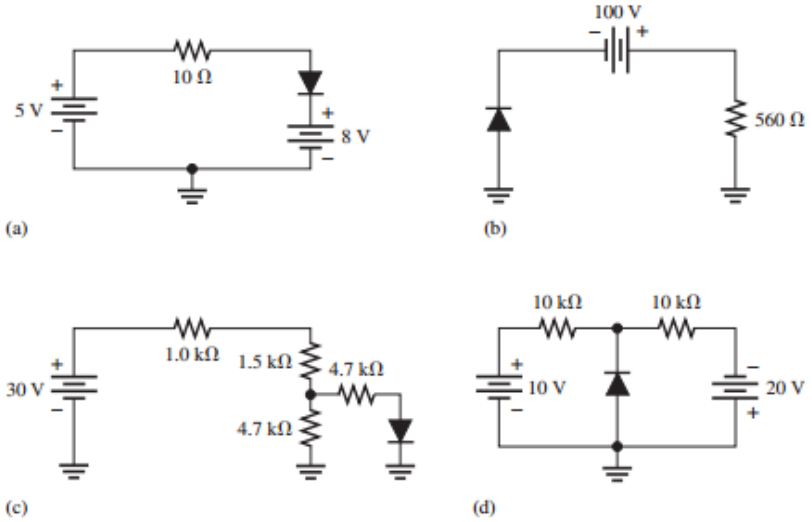

Figure 5

c) Determine the peak-to-peak ripple voltage, the dc output voltage and the ripple factor in Figure 6. The transformer has a 36 V rms secondary voltage rating, and the line voltage has a frequency of 60 Hz. [4+2+1 Marks]

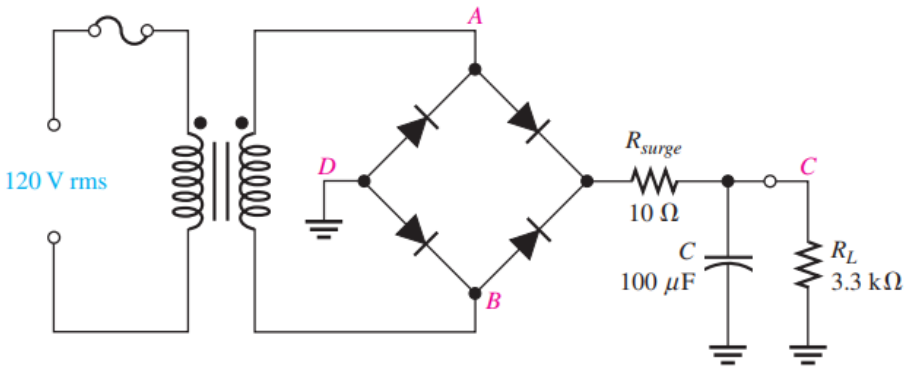

Figure 6

d) Draw the output waveform of the circuit in Figure 7. Assume that the RC time constant is much greater than the period of the input signal. [4 Marks]

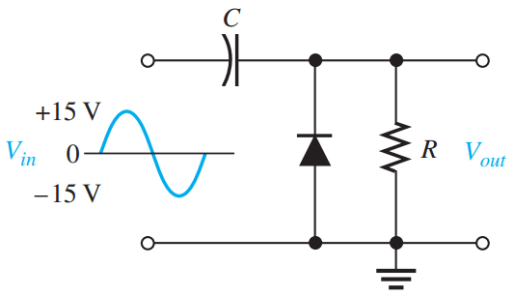

Figure 7

[Total = 25 Marks]

Question 3

a) A certain *p*-channel JFET has a $V_{GS(off)} = 6$ V. What is the value I_D when $V_{GS} = 8$ V? [2 Marks]

b) The JFET in Figure 8 has $V_{GS(OFF)} = -4$ V. Assume that you increase the supply voltage, V_{DD}, beginning at zero until the ammeter reaches a steady value. What value does the voltmeter read at this point and why? [3 Marks]

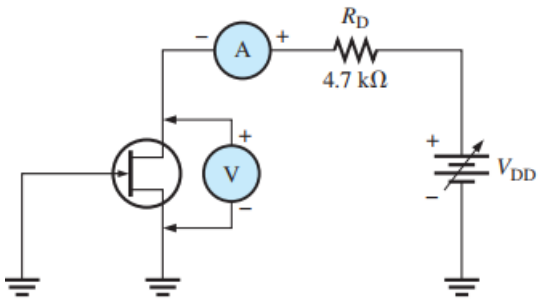

Figure 8

c) Using the curve in Figure 9, determine the value of R_S required for a 9.5 mA drain current. [4 Marks]

d) Determine the total input resistance in Figure 9, $I_{GSS} = 20$ nA at $V_{GS} = -10$ V. [2 Marks]

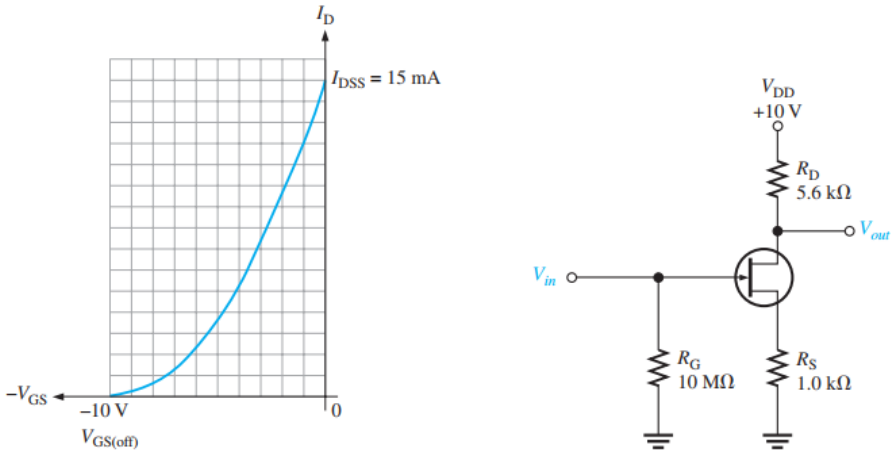

Figure 9

e) Find V_{GS} and V_{DS} for each of the E-MOSFETs in Figure 10. Datasheet information is listed with each circuit. [10 Marks]

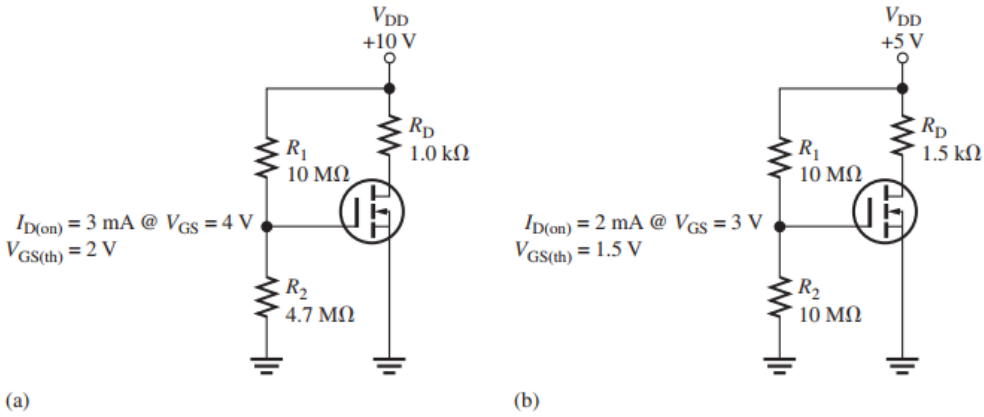

Figure 10

f) Determine the actual gate-to-source voltage in Figure 11 by taking into account the gate leakage current, I_{GSS}. Assume that I_{GSS} is 50 pA and I_D is 1 mA under the existing bias conditions. [4 Marks]

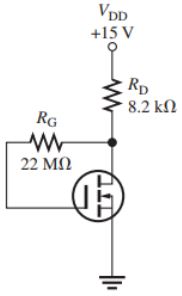

Figure 11

[Total = 25 Marks]

Question 4

a) Find V_{CE} of the transistor below. You may assume that V_{BE} of the transistor is 0.7 V and β_{DC} is very high. [5 Marks]

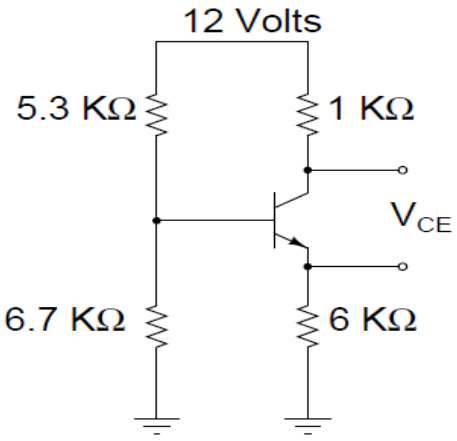

Figure 12

b) With aid of diagrams, explain how a differential amplifier is able to reject common mode input signals and yet amplify differential mode input signals. [8 Marks]

c) (i) Determine the total input resistance of the emitter follower in the Figure 13 below. Assume that βac = 175 and the capacitive reactances are negligible at the frequency of operation.

[4 Marks]

ii) Also find the voltage gain, the current gain and the power gain in terms of the power delivered to the load, R_L. [1 + 4 + 3 Marks]

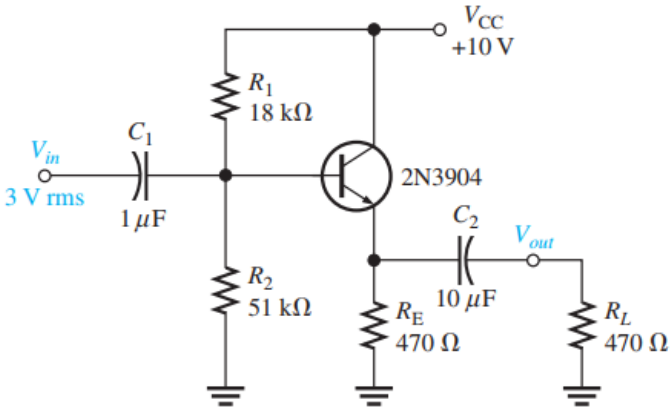

Figure 13

[Total = 25 Marks]

Question 5

a) i) What is the purpose of the voltage follower in the circuit below? [2 marks]

ii) Calculate the gain of this circuit. [1 marks]

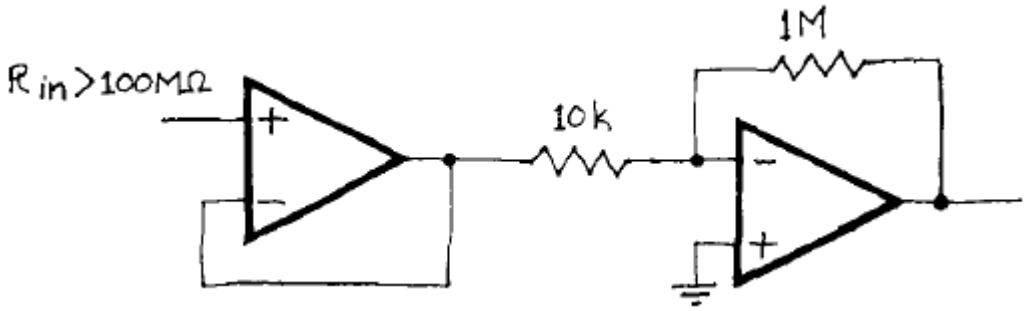

Figure 14

b) Determine the output waveform for the figure below [12 Marks]

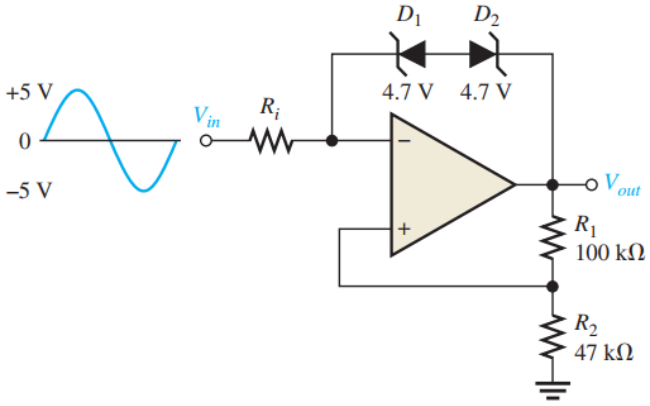

Figure 15

c) For the Wien-Bridge oscillator in Figure 16, calculate the value of R_f, assuming that the internal drain-source resistance r'_{ds} of the JFET is 350 Ω when oscillations are stable. [3 Marks]

d) Find the frequency of oscillation for the Wien-Bridge oscillator in Figure 16. [2 Marks]

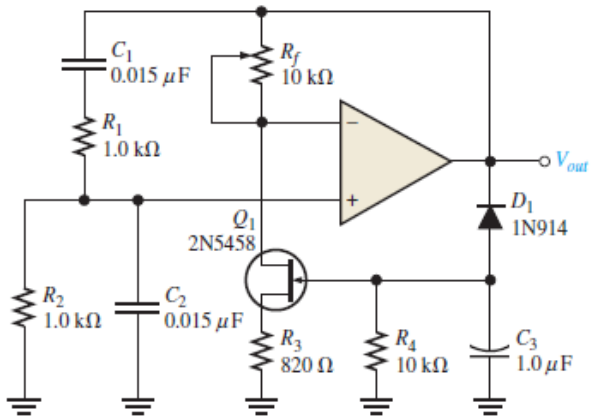

Figure 16

e) Explain how the automatic gain control of the circuit in Figure 16 above works. [5 Marks]

[Total = 25 Marks]