NATIONAL UNIVERSITY OF LESOTHO

B.Eng/B.Sc SUPPLEMENTARY EXAMINATIONS

EE4401 – Digital Circuit Design

AUGUST 2023 **TIME: 3 HOURS**

INSTRUCTIONS: Answer any 4 questions

: Begin answering each question on a new sheet

: Under each question answer the sub questions in the chronological order

TOTAL MARKS: 100

IMPORTANT FORMULAE:

Average Power: $P_{D(avg)} = I_{CC(avg)} * V_{CC}$

Average Current: $I_{CC(avg)} = 0.5(I_{CCL} + I_{CCH})$

Question 1

a) If A = 1101_2 and B = 0101_2 and they are to be added with carry look ahead adder, show how C_1, C_2, C_3 , and C_4 will be produced using the generate and the propagate functions and calculate their values. [8 Marks]

b) Implement the following functions using NOR logic

F = XY + XZ + $\bar{X}$YZ [3 Marks]

G = $\overline{X + Y}$ [1 Mark]

c) The R-2R ladder DAC is connected to a 12V supply where R = 6 kΩ; and R_F = 18 kΩ. Predict the analogue signal value if the input digital word is 0011100100. [6 Marks]

d) Generally, what elements make up a configurable logic block (CLB) in an FPGA? What elements make up a logic module? [4 Marks]

e) Determine the output the Some OF Products (SOP) expression of the LUT for the internal conditions shown in the figure below [3 Marks]

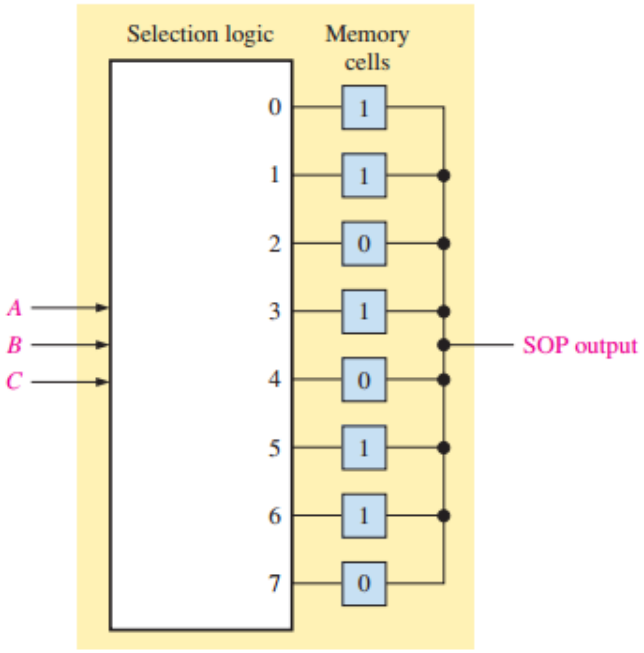

Figure 1

[Total = 25 Marks]

Question 2

a) A remote digital receiver module designed for receiving BDC code information must have an error detection circuit. The error detection circuit's output Z must be high whenever an invalid BCD code [$C_3 – C_0$] is received (i.e. [$C_3 – C_0$] > 1001).

i) Design a minimal combinational error detection circuit for the receiver. [8 Marks]

ii) Implement the error detection circuit using NAND gates only. [5 Marks]

iii) Implement the error checking circuit using **only one** 8-to1 line multiplexor. N.B don't draw the multiplexor at the gate level, use only a block diagram that represents that multiplexor. [6 Marks]

b) What is the difference between PAL, CPLD and FPGA? [6 Marks]

[Total = 25 Marks]

Question 3

a) Implement **Synchronous** 3-bit counter using D flip-flops [9 Marks]

b) Indicate how you will use the JK Flip-Flop to act as D flip-flop. [3 Marks]

c) Consider a presentable clock divider shown in the figure below. If the clock divider's input is 2 kHz, its output should vary depending on the input D[1:0] as shown in the table below.

D1	D0	Output Frequency [Z]
0	0	1 kHz
0	1	500 Hz
1	0	250 Hz
1	1	125 Hz

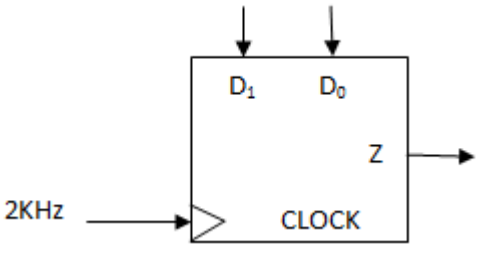

Figure 2

Use 2-bit counters and 2-to-1 line multiplexors only, to design a presentable counter. [8 Marks]

d) Draw a 4 bit serial-in serial-out shift register using JK flip-flops [5 Marks]

[Total = 25 Marks]

Question 4

a) A flash-ADC shown in Figure 3 is to be used in a data –acquisition industrial application. The analogue voltage output of the sensor V_A is proportional to the pressure being monitored.

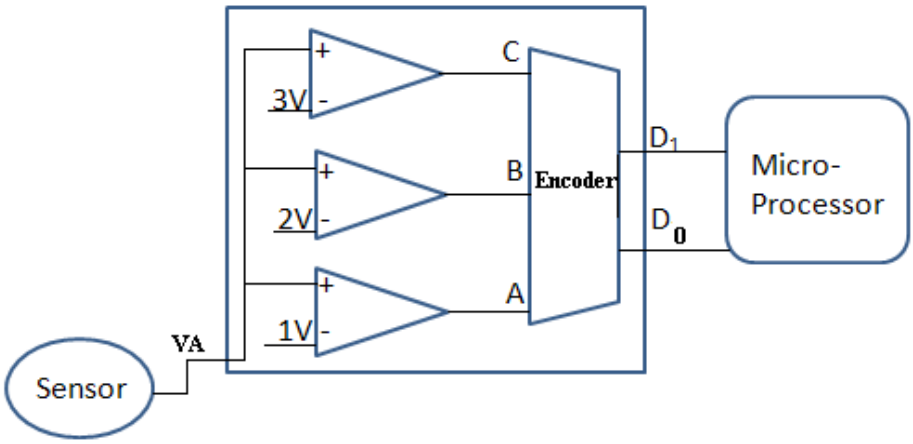

Figure 3

(i) Complete the design of a flash-ADC in Figure 3 by designing an encoder that will provide a resolution of 1 volt. That is, when V_A is within [0,1) volts then the $[D_1D_0] = 00$, when V_A is in the interval [1,2) volts then $[D_1D_0] = 01$ etc. [10 Marks]

(ii) Assume that the propagation delay of analogue voltage comparators is negligible and the existence of 2-input NOR-gates with a maximum propagation delay of 10ns. Implement the encoder design of (i) above using NOR-gates only and estimate conversion-time of the flash-ADC. [7 Marks]

b) A vehicle uses a speed sensor and a 10-bit SAR-ADC for its digital speed indication. The transducer sensitivity is 90 mV/kph and the ADC clock frequency is 89 kHz. Assuming that V ref = 12 V (full-scale deflection) and the vehicle speed is 80 kph (kilometre per hour) find the converter binary output. [8 Marks]

[Total = 25 Marks]

Question 5

a) Two different logic circuits have the characteristics shown in the figure below.

i) Which circuit has the best LOW-state dc noise immunity? Which circuit has the best HIGH-state dc noise immunity? [5 Marks]

ii) Which circuit can operate at higher frequencies? [5 Marks]

iii) Which circuit draws the most supply current? [3 Marks]

	Circuit *A*	Circuit *B*
V_{supply} (V)	6	5
V_{IH}(min) (V)	1.6	1.8
V_{IL}(max) (V)	0.9	0.7
V_{OH}(min) (V)	2.2	2.5
V_{OL}(max) (V)	0.4	0.3
t_{PLH} (ns)	10	18
t_{PHL} (ns)	8	14
P_D (mW)	16	10

Figure 4

b) A certain logic family has the following voltage parameters

V_{IH}(min) = 3.5 V V_{IL}(max) = 1.0 V

V_{OH}(min) = 4.9 V V_{OL}(max) = 0.1 V

i) What is the largest positive-going noise spike that can be tolerated? [2 Marks]

ii) What is the largest negative-going noise spike that can be tolerated? [2 Marks]

c) Draw a diagram of a TTL NOR gate [6 Marks]

d) Determine the output of the array in the figure below [2 Marks]

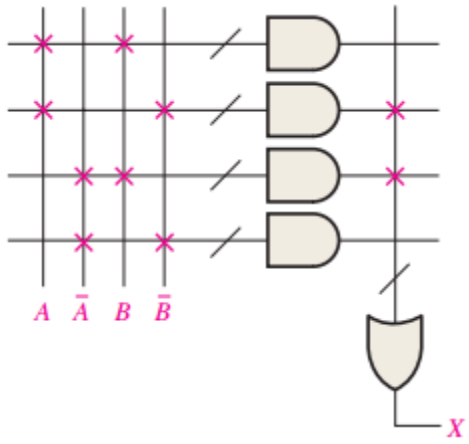

Figure 5

[Total = 25 Marks]